The following Listing of Claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) An integrated circuit device comprising:

a substrate;

a first insulation layer on the substrate;

a contact pad disposed in the first insulation layer in direct contact with the substrate;

a second insulation layer on the first insulation layer;

a conductive pattern in the second insulation layer and positioned on one side of the contact pad; ~~and~~

a conductive plug extending through the second insulation layer adjacent the conductive pattern to contact the contact pad ~~and self-aligned to the conductive pattern~~; and

an insulating film disposed between a sidewall of the conductive plug and sidewalls of the conductive pattern and the second insulation layer.

2. (Original) The device according to Claim 1, wherein the second insulation layer comprises an oxide, and wherein the conductive pattern comprises tungsten.

3. (Canceled)

4. (Currently Amended) The device according to Claim [[3]] 1, wherein the insulation film comprises silicon oxide and/or silicon nitride.

5. (Original) The device according to Claim 4, wherein the insulation film has a thickness of about 50Å to about 600Å.

6. (Original) The device according to Claim 1, wherein the conductive pattern comprises a bit line.

7. (Original) The device according to Claim 1, wherein the conductive pattern comprises a damascene pattern disposed in a trench in the second insulation layer.

8. (Original) The device according to Claim 1:

wherein the first insulation layer comprises a silicon oxide, a high density plasma oxide, a high temperature oxide, a middle temperature oxide, a tetraethyl ortho-silicate, a polysilazane, a flowable oxide and/or a black diamond material; and

wherein the second insulation layer comprises a silicon oxide, a high density plasma oxide, a high temperature oxide, a middle temperature oxide, a tetraethyl ortho-silicate, a polysilazane, a flowable oxide and/or a black diamond material.

9. (Currently Amended) The device according to Claim 1, further comprising a glue layer disposed between the conductive pattern and the second insulation layer and between the conductive pattern and the insulating film.

10. (Original) The device according to Claim 9, wherein the glue layer comprises titanium nitride, tantalum nitride or boron nitride.

11. (Original) The device according to Claim 9, wherein the glue layer has a thickness less than about 300Å.

12. (Original) The device according to Claim 1, wherein the conductive pattern comprises tungsten, tantalum nitride, titanium nitride, cobalt, nickel and/or aluminum.

13. (Currently Amended) The device according to Claim 1, further comprising a third insulation layer on the second insulation layer and the conductive pattern, and wherein the conductive plug and the insulating film ~~extends~~ extend through the second and third insulation layers.

14. (Original) The device according to Claim 13, wherein the third insulation layer comprises a silicon oxide, a high density plasma oxide, a tetraethyl ortho-silicate, a middle temperature oxide and/or a high temperature oxide, a polysilazane, a flowable oxide and/or a black diamond material.

15. (Original) The device according to Claim 1:

wherein the conductive pattern comprises tungsten, tantalum nitride, aluminum, nickel, or cobalt; and

wherein the conductive plug comprises tungsten, titanium nitride, tantalum nitride and/or polysilicon.

16. (Currently Amended) An integrated circuit memory device comprising:

a substrate having a source/drain region therein;

a first insulation layer on the substrate;

a storage node contact pad disposed in the first insulation layer and directly contacting the source/drain region;

a second insulation layer on the first insulation layer;

first and second damascene bit lines disposed in respective trenches in the second insulation layer on opposite sides of the storage node contact pad;

a conductive plug extending through the second insulation layer between the first and second damascene bit lines to contact the storage node contact pad~~, the conductive plug self-aligned to the first and second bit lines~~;

respective insulating films disposed between respective sidewalls of the conductive plug and sidewalls of the bit lines and the second insulation layer; and

a capacitor disposed on the conductive plug.

17. (Original) The memory device according to Claim 16, wherein the second insulation layer comprises an oxide, and wherein the first and second bit lines each comprise tungsten.

18. (Canceled)

19. (Original) The memory device according to Claim 16:

wherein the first insulation layer comprises a silicon oxide, a high density plasma oxide, a high temperature oxide, a middle temperature oxide, a tetraethyl ortho-silicate, a polysilazane, a flowable oxide and/or a black diamond material; and

wherein the second insulation layer comprises a silicon oxide, a high density plasma oxide, a high temperature oxide, a middle temperature oxide, a tetraethyl ortho-silicate, a polysilazane, a flowable oxide and/or a black diamond material.

20. (Currently Amended) The memory device according to Claim 16, further comprising respective glue layers disposed between respective ones of the first and second bit lines and the second insulation layer and the insulating films.

21. (Original) The memory device according to Claim 20, wherein the glue layers each comprises titanium nitride, tantalum nitride or boron nitride.

22. (Original) The memory device according to Claim 16, wherein the first and second bit lines each comprises tungsten, tantalum nitride, titanium nitride, cobalt, nickel and/or aluminum.

23. (Currently Amended) The memory device according to Claim 16, further comprising a third insulation layer on the second insulation layer and the first and second bit lines, wherein the conductive plug and the insulating films ~~extends~~ extend through the second and third insulation layer, and wherein the capacitor is disposed on the third insulation layer.

24. (Original) The memory device according to Claim 23, wherein the third insulation layer comprises a silicon oxide, a high density plasma oxide, a tetraethyl ortho-silicate, a middle temperature oxide and/or a high temperature oxide, a polysilazane, a flowable oxide and/or a black diamond material.

25. (Original) The memory device according to Claim 16:

wherein the first and second bit lines each comprise tungsten, tantalum nitride, aluminum, nickel, or cobalt; and

wherein the conductive plug comprises tungsten, titanium nitride, tantalum nitride and/or polysilicon.

26-51. (Canceled)